RESPONSE

This Response is filed in response to the Office Action mailed on July 21, 2004. In the Office Action, Claims 1-4, 7-15, and 19-26 are pending in the Application. Claims 1-4, 7-15, and 19-26 stand rejected.

Amendment as a Matter of Form

Claim 14 was amended as a matter of form to include commas at the appropriate locations, specifically after "generating," and after "elements." Claim 14 was also amended as a matter of form to change "fault tolerant" to "fault-tolerant" i.e., hyphenating the combination. No new matter has been added.

Rejections Under 35 U.S.C. §112

Claim 24 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to distinctly claim the subject matter. Claim 24 has been amended to remove "the" in reference to "packets." No new matter has been added. Support for the amendment may be found in the previously presented claim 24, as well as in paragraph 0066 of the specification. Therefore, the Applicants respectfully submit that claim 24 is in condition for allowance.

Rejections Under 35 U.S.C. §103

Claims 1-4, 7-15, and 19-26 were rejected under 35 U.S.C. §103(a) as being unpatentably obvious over U.S. Patent No. 6,643,764 to Thorson et al. (hereinafter "Thorson") in view of U.S. Patent No. 5,446,726 to Rostoker et al. (hereinafter "Rostoker") and U.S. Patent No. 3,783,250 to Fletcher et al. (hereinafter "Fletcher"). The Applicants respectfully traverse the rejections as applied to the original and the amended claims, and submit that none of the references, alone or in combination, teach or suggest the claimed invention.

Thorson

Thorson is directed to "routing messages on multiple links in multiprocessor computer systems." Col. 1, lines 9-10. Thorson addresses the need for improved infrastructure in "[m]ultiprocessor computer systems having up to hundreds or thousands of processing element

nodes . . . typically referred to as massively parallel processing (MPP) systems." Col. 1, lines 19-22 and lines 51-52.

In particular, Thorson teaches:

> [A] multiprocessor computer system having a plurality of processing element nodes and an interconnect network interconnecting the plurality of processing element nodes. An interface circuit is associated with each one of the plurality of processing element nodes. The interface circuit has a lookup table having n-number of routing entries for a given destination node. Each one of the n-number of routing entries [is] associated with a different class of traffic.

Col. 1, lines 55-63 (emphasis added). Thorson's multiprocessor system "provides redundant paths." Col. 5, lines 66-67. "The network traffic is routed according to class." Abstract.

As the Examiner put forth in the Office Action dated July 21, 2004, Thorson states, "[a]nother way the infrastructure affects performance of an MPP system is in the level of fault tolerance provided by the infrastructure," thus indicating a need for "fault tolerance." Col. 1, lines 43 – 44. Thorson then continues, "[f]or example, if a segment of the communication path fails, the MPP is unable to continue normal operation unless an alternate or redundant path is provided" and "[f]urther more, [sic] switching traffic to the redundant path is often difficult." Col. 1, lines 44 – 49. Thus, Thorson discloses a desire for fault-tolerance in network traffic communication handling between processing nodes.

In summary, Thorson suggests routing traffic by class between processing element nodes in a multiprocessor computer system. Thorson also expresses a desire for network and path fault-tolerance between processing elements.

Rostoker

Rostoker is directed to "[a]n asynchronous transfer mode (ATM) processing system or termination unit embodying the present invention [that] is implemented on a single integrated circuit chip," and is "capable of executing or facilitating almost any congestion control algorithm imaginable." Col. 3, lines 25-28; Col. 5, lines 21-23.

In particular, Rostoker teaches:

> "An adaptive error detection and correction apparatus for an Asynchronous Transfer Mode (ATM) network device comprises a sensing unit for sensing a congestion condition in the ATM network and a global pacing rate unit for adaptively reducing a maximum allowable transmission ratio of ATM cells containing information to idle ATM cells in response to a sensed congestion condition," where "the invention includes embodying the present ATM interconnect device as a hub, bridge, uniprotocol or multi-protocol router, or in any other configuration regarding ATM termination, switching or routing."

Abstract; Col. 3, line 65 – Col. 4, line 1.

As illustrated in Figure 1, Rostoker's invention 50 is connected on one side to a router 20, allowing data to pass through Ethernet hubs 22, 24, and eventually to workstations 16. Col. 8, lines 50 - 54. Rostoker's invention is also connected through an ATM link 18 to a Public Service Telephone Network (PSTN). Col. 8, lines 49 – 50. The router 26, absent Rostoker's device 50, connects to the PSTN 12 via a non-ATM WAN connection 28. Col. 8, line 63 - 64.

In summary, Rostoker teaches a congestion control apparatus connected to a router on one side and an ATM link on the other. A router without Rostoker's device may connect to a PSTN through a WAN connection.

Fletcher

Fletcher is directed to a "computer system using adaptive voting to tolerate failures and operate in a fail-operational, fail safe manner," using "four-way voting, wherein each computer module is performing the same operation, with one or more control apparatus providing voting or failure analysis to determine operation/failure status of the computer modules." Abstract; Col. 1, lines 58-62.

In particular, Fletcher teaches "[a] computer system S includ[ing] four computers: a computer A, a computer B, a computer C, and a computer D. Each of the computers A, B, C, and D are general purpose digital computers and are connected to individual input/output (I/O) data busses 10, 20, 30, and 40, which interface with local processors of external subsystems." Col. 2, lines 47 – 55. Additionally, with respect to Fletcher's invention interfacing with the external subsystems, "[computer-to-external subsystem] channel communications are bit serial-word serial and provide data and commands from the computer module to the associated I/O data

bus 10, 20, 30, or 40, as the case may be that connects the computer system S to various external subsystems. The transfer of data over the [computer-to-external subsystem] channel is under control of the [Input/Output Processor (IOP)], and external subsystems ... communicate with the IOP only when permitted to do so by the IOP." Col. 4, lines 14 – 23.

In summary, Fletcher teaches a computer system that utilizes adaptive voting across local buses to detect failures, where the communications to external subsystems across those buses occur only when permitted by the Input/Output Processor.

Rejection of Claim 1 over Thorson in View of Rostoker and Fletcher

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one or ordinary skill in the art, to modify the references or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on disclosure."
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> *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) as quoted in the MPEP, § 706.02(j)

Thorson, Rostoker, and Fletcher do not teach or suggest, alone or in combination, the elements recited in the previously presented claim 1. Specifically, the references do not teach "a plurality of data processing elements executing substantially identical instruction streams substantially simultaneously;" "an I/O node in communication with at least one of the plurality of data processing elements;" or "a switching fabric communicating transactions asynchronously between at least one of the plurality of data processing elements and the I/O node."

The Examiner asserts that it would be obvious to one skilled in the art to combine Thorson with Fletcher to achieve fault tolerance, i.e., "Thorson does show a desire to increase the fault tolerance of the infrastructure (See Col. 1, lines 42-50)" and "it would be obvious to one of ordinary skill in the art at the time of [the] invention to do because ... the redundant processors allow continued operation in the event of a failure." Office Action, Page 3, paragraph 6. The Applicants respectfully disagree. Though Thorson expresses a desire for "fault tolerance," the fault tolerance Thorson desires is for network and path fault-tolerance. Thorson specifically

states, "[a]nother way the infrastructure affects performance of an MPP system is in the level of fault tolerance provided by the infrastructure. For example, if a segment of the communication path fails, the MPP is unable to continue normal operation unless an alternate or redundant path is provided" and "[f]urther more, [sic] switching traffic to the redundant path is often difficult." Col. 1, lines 44 – 49. Fletcher provides a different type of fault tolerance, that is, computer module fault-tolerance. Specifically,

> "In the operation of the present invention, the computer system S may be operated in a variety of interconnection modes depending upon the desired degree of redundancy in the processing of the data by such computer system. ... The votin [sic] taking place is adaptive in that once an error has been detected in a computer module or the control; apparatus P associated therewith, output signals and data and commands from such computer module are disregarded in subsequent voting..."

Fletcher, Col. 39, lines 48-59. Thus, it would not be obvious to one skilled in the art to combine Thorson with Fletcher because Thorson, seeking path fault tolerance between computing modules, shows no motivation to combine with an invention that provides computer module fault tolerance. Specifically, Thorson only deals with providing fault tolerance for communication paths, but has nothing to do with fault tolerance for multiple processors. Accordingly, Thorson, alone or in combination with Fletcher, does not disclose the elements of claim 1.

The Examiner also states in the Office Action that it would be obvious to one skilled in the art to combine Thorson and Rostoker to derive the elements of previously presented independent claim 1. Specifically, the Examiner puts forth that because Thorson presents a desire to increase network bandwidth, it would be obvious to one skilled in the art to combine Thorson with Rostoker. The Examiner states that combining Thorson with Rostoker is obvious because, "the ATM protocol is highly advantageous in that it enables high speed transmissions (see Rostoker, Col. 2, lines 22-25), thus allowing higher bandwidth ..." Office Action, Page 4, paragraph 6. The Applicants respectfully disagree. Rostoker teaches a traffic congestion controller chip to be installed on an ATM router on an existing ATM network. This imposes that an ATM network be present for Rostoker's invention to function. As depicted in Rostoker's Figure 1, a router 26, as is disclosed in Thorson, may be connected to a PSTN using a non-ATM WAN connection. Rostoker's invention 50, however, utilizes an ATM connection to the PSTN.

None of Rostoker's depictions illustrate incorporating an ATM traffic congestion apparatus on a non-ATM network. Additionally, Rostoker does not teach or suggest multiprocessor fault tolerance, specifically "a plurality of data processing elements executing substantially identical instruction streams substantially simultaneously," as is claimed in previously presented independent claim 1. Likewise, nowhere in Thorson is an ATM link or an ATM traffic congestion apparatus disclosed, suggested, or mentioned. Therefore, Thorson's invention shows no motivation to combine with ATM technology, nor does Rostoker's apparatus show a motivation to combine with multiprocessor fault tolerance. A general statement of desire to increase bandwidth in Thorson does not teach or suggest utilizing an ATM network to do so. Thus, the Applicants respectfully submit that Thorson does not teach or suggest, alone or in combination with Rostoker, the elements of independent claim 1.

Additionally, the Rostoker and Fletcher references demonstrate a lack of motivation to combine because the references teach away from one another. Specifically, Rostoker teaches an apparatus on an ATM network, i.e., "[a]n adaptive error detection and correction apparatus for an Asynchronous Transfer Mode (ATM) network." Abstract. Fletcher teaches a voting mechanism between computers connected via local buses, not networks. Col. 2, lines 47 – 55. As described above, Fletcher's invention teaches a communication system whereby the IOP controls communications with the external subsystems across a local bus and that the "external subsystems ... communicate with the IOP only when permitted to do so by the IOP." Col. 4, lines 20 – 23. Synchronized communications between the external subsystems and the IOP are at odds with the asynchronous nature of an ATM network, and thus Rostoker's congestion control apparatus.

Therefore, the Applicants respectfully submit that it would not be obvious to one skilled in the art to combine Thorson, Rostoker, and Fletcher, and that the aforementioned references do not teach or suggest, alone or in combination, the elements of the previously-presented independent claim 1. Further, the Applicants submit that claims 2-4 and 7-13, which depend on claim 1, and include all of the limitations therein, are also patentable over Thorson in view of Fletcher and Rostoker.

Rejection of Claim 14 over Thorson in View of Rostoker and Fletcher

As discussed above with respect to claim 1, Thorson, Rostoker, and Fletcher, alone or in combination, do not teach or suggest the elements of currently amended independent claim 14. Namely, the references do not teach, "generating, by a plurality of data processing elements, identical transactions each having an I/O node address; and communicating the identical transactions asynchronously on a switching fabric to the I/O node–identified by the I/O node address." Thorson teaches a multiprocessor apparatus, Rostoker teaches an ATM traffic congestion control apparatus, and Fletcher teaches an adaptive voting computer system.

As stated above, there is no motivation to combine Thorson with Rostoker, i.e., no ATM network is disclosed or suggested in Thorson and no desire for multiprocessor fault-tolerance ("generating, by a plurality of data processing elements, identical transactions") is disclosed or suggested in Rostoker. There is also no motivation to combine Thorson and Fletcher since Thorson suggests a desire for network fault tolerance whereas Fletcher teaches multiprocessor fault-tolerance. Additionally, Rostoker and Fletcher teach away from one another since a network of any kind is absent from Fletcher and Fletcher also requires synchronous communication with external subsystems. Col. 4, lines 14 – 23. Synchronous communication is directly at odds with "communicating the identical transactions asynchronously on a switching fabric" as is claimed in currently amended claim 14.

Thus, the Applicants respectfully submit that, since Thorson, Rostoker, and Fletcher do not teach or suggest, in combination or alone, the elements of claim 14, claim 14 is patentable over Thorson, in view of Rostoker and Fletcher. Further, the Applicants submit that claims 15 and 19, which depend on claim 14 and include all of the limitations therein, are also patentable in view of the aforementioned references.

Rejection of Claim 20 over Thorson in View of Rostoker and Fletcher

As discussed above with respect to claim 1, Thorson, Rostoker, and Fletcher, alone or in combination, do not teach or suggest the elements of previously presented independent claim 20. Namely, the references do not teach, "a plurality of data processing elements executing substantially identical instruction streams substantially simultaneously; a voting module in

communication with the plurality of data processing elements for comparing the I/O instructions associated with at least two of the plurality of data processing elements; an I/O node in communication with the voting module; and a switching fabric communicating transactions asynchronously between the voting module and the I/O node." Thorson teaches a multiprocessor apparatus, Rostoker teaches an ATM traffic congestion control apparatus, and Fletcher teaches an adaptive voting computer system.

As stated above, there is no motivation to combine Thorson with Rostoker, i.e., no ATM network is disclosed or suggested in Thorson and no desire for multiprocessor fault-tolerance ("a plurality of data processing elements executing substantially identical instruction streams substantially simultaneously") is disclosed or suggested in Rostoker. Though the Examiner asserts that Thorson combined with Fletcher additionally teaches "a voting module in communication with the data processing elements for comparing I/O instructions associated with at least two of the plurality of data processing elements," the Applicants respectfully submit that, as stated before, Thorson indicates a desire for network fault tolerance, not computing module ("data processing element") fault tolerance. Office Action, page 8, paragraph 17. Therefore, there is still no motivation to combine Thorson with Fletcher. As described above, Rostoker and Fletcher teach away from one another since a network of any kind is absent from Fletcher and Fletcher also requires synchronous communications with external subsystems. Col. 4, lines 14 – 23. Synchronous communication is directly at odds with "a switching fabric communicating transactions asynchronously between the voting module and the I/O node" as claimed in previously presented claim 20.

Thus, the Applicants respectfully submit that, since Thorson, Rostoker, and Fletcher do not teach or suggest, in combination or alone, the elements of claim 20, claim 20 is patentable over Thorson in view of Rostoker and Fletcher. Further, the Applicants submit that claims 21-26, which depend on claim 20 and include all of the limitations therein, are also patentable in view of the aforementioned references.

Therefore, in light of the foregoing reasons, the Applicants respectfully request that the rejections under 35 U.S.C. §103 be reconsidered and withdrawn.

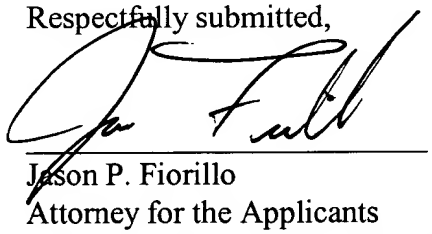
SUMMARY

Claims 1-4, 7-15, and 19-26 are pending in the application. Claims 1-4, 7-15, and 19-26 stand rejected. The Applicants request that the Examiner reconsider the application and claims in light of the foregoing Amendment and Response, and respectfully submit that the pending claims are in condition for allowance.

If, in the Examiner's opinion, a telephonic interview would expedite the favorable prosecution of the present application, the undersigned attorney would welcome the opportunity to discuss any outstanding issues, and to work with the Examiner toward placing the application in condition for allowance.

Applicants believe that no additional fees are necessitated by the present Amendment. However, in the event that any additional fees are due, the Commissioner is hereby authorized to charge any such fees to Attorney's Deposit Account No. 20-0531.

Respectfully submitted,



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